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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/954,713	09/18/2001	Seiji Ishikawa	782_183	7609

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EXAMINER	
KWOK, HELEN C	

ART UNIT	PAPER NUMBER
2856	

DATE MAILED: 05/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/954,713	Applicant(s) Ishikawa et al.
	Examiner H. Kwok	Art Unit 2856

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Apr 2, 2003* .

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-16 and 18-21* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-16 and 18-21* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-16 and 18-21 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,783,748 (Otani).

With regards to claims 1-7, Otani discloses a semiconductor sensor package comprising, as illustrated in Figures 1-2 and 24, a vibrating element 1a; a vibration element supporting member 1b for supporting the vibration element; a circuit board 1 (i.e. a HIC board) for supporting the vibration element; a semiconductor integrated circuit chip (since the circuit board is a HIC board, circuit chips are provided on the board) for controlling signals from the vibration element; a base and a lid to form a can-package 3 for securing the vibrating element, the supporting member, the circuit board and the circuit chip such that the circuit chip is mounted on the circuit board by bonding (i.e. flip-chip or bare-die, which are well known as provided in the specification of the present application) and the vibration element is mounted to the circuit chip by the supporting member. Furthermore, the vibration element and circuit chip are arranged to

be overlapped and parallel with each other. (See, column 1, lines 11-52 and column 5, line 36 to column 6, line 60).

With regards to claims 8-16 and 18-21, the claims are commensurate in scope with claims 1-7 and are rejected for the same reasons as set forth above.

3. Claims 1-16 and 18-21 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 6,094,984 (Asano et al.).

With regards to claims 1-7, Asano et al. discloses a semiconductor sensor package comprising, as illustrated in Figures 2-3 and 12, a vibrating element 2; a vibration element supporting member for supporting the vibration element (not shown; however, one knows a support is used to mount the vibrating element); a circuit board 3 for supporting the vibration element; a semiconductor integrated circuit chip E for controlling signals from the vibration element; a base 5 and a lid 7 to form a can-package for securing the vibrating element, the supporting member, the circuit board and the circuit chip such that the circuit chip is mounted on the circuit board by bonding (i.e. flip-chip or bare-die, which are well known in the art as disclosed in the specification of the present application) and the vibration element is mounted to the circuit chip by the supporting member. Furthermore, the vibration element and circuit chip are arranged to be overlapped and parallel with each other. (See, column 3, line 61 to column 4, line 31).

With regards to claims 8-16 and 18-21, the claims are commensurate in scope with claims 1-7 and are rejected for the same reasons as set forth above.

Response to Amendment

4. Applicant's arguments filed April 2, 2003 have been fully considered but they are not persuasive. .

Applicants argue that the references, Otani and Asano et al., do not teach the "semiconductor integrated circuit chip mounted on the circuit board" and "the vibration element is mounted on the semiconductor integrated circuit chip" (namely mounted on any of the individual chip components), as presently claimed in claim 1.

The Examiner believes the references, Otani and Asano et al., do suggest the semiconductor integrated circuit chip mounted on the circuit board and the vibration element is mounted on the semiconductor integrated circuit chip. According to Otani, as mentioned in the last Office Action, a hybrid integrated circuit (HIC) board 1a (i.e. circuit board) contains and provides semiconductor integrated circuit chip on the circuit board and these integrated circuit chip are mounted on the circuit board. (A definition for the word "hybrid integrated circuit" and "integrated circuit" is provided). Furthermore, the vibrating element 1a is mounted on the semiconductor integrated circuit chip by means of a supporting member 16, as observed in Figure 1. As presented in claim 1, the vibration element is mounted on the integrated circuit chip by means of the supporting member and this is what the Otani reference teaches. There is no

claim language in the claim stating the vibration element is mounted on the integrated circuit chip or any of the individual chip components as argued in the Amendment. Moreover, Asano et al. teaches circuit elements E mounted on a circuit board 3, as observed in Figure 2. Also, as observed in Figure 2, a vibrating element 2 is mounted on the integrated circuit chip E for the same reasons as provided above. Also, as presented and observed in Figure 1 of the present Application, there is no direct mounting of the vibrating element to the integrated circuit chip. There is a supporting member between these two elements. Therefore, the references, Otani and Asano et al., do teach the "semiconductor integrated circuit chip mounted on the circuit board" and "the vibration element is mounted on the semiconductor integrated circuit chip" for the reasons set forth above.

Applicants further argue that the references, Otani and Asano et al., do not teach the "a lid and the circuit board define a space in which the vibration element and the vibration element supporting member is enclosed", as presently claimed in claim 8.

The Examiner believes the references, Otani and Asano et al., suggest a lid and the circuit board define a space in which the vibration element and the vibration element supporting member is enclosed. According to Otani, as observed in Figure 8 and described in column 7, lines 39-63, a lid 16 is secured to the circuit board 9 to create a space 16b to install the vibration element 9a and supporting member within the space 16b. Asano et al. also suggest, as illustrated in Figure 16, a lid 550 is secured to the circuit board 530 to create a space S to install the vibration element 520 and supporting member within the space S. Therefore, Otani and Asano et

al., do not teach a lid and the circuit board define a space in which the vibration element and the vibration element supporting member is enclosed for the reasons set forth above.

Applicants further argue that the references, Otani and Asano et al., do not teach the "vibration element and integrated circuit chip are arranged to be overlapped with each other", as presently claimed in claim 18.

The Examiner believes the references, Otani and Asano et al., suggest the vibration element and integrated circuit chip are arranged to be overlapped with each other. According to Otani, as observed in Figure 21, resistors and conductors, which are components of integrated circuit chip, are positioned under a portion of the vibration element and are overlapping one another since overlapping is usually defined as to occupy the same area in part or to have something in common. Furthermore, Asano et al. also teaches the vibration element 2 and integrated circuit chip E overlapping one another. As observed in Figure 2, the vibration element 2 occupies a common area with the integrated circuit chip E. Therefore, Otani and Asano et al., do not teach the vibration element and integrated circuit chip are arranged to be overlapped with each other as set forth above.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Kwok whose telephone number is (703) 308-8149.

Helen C. Kwok
Art Unit 2856

hck
May 7, 2003